

ABSTRACT

A non-volatile memory cell comprising a latch circuit (1) which comprises a first node (6) and a second node (7) and latches complementary data set in the first node (6) and the second node (7), a first switching element (4) which connects the first node (6) and a first data input/output line (2), a second switching element (5) which connects the second node (7) and a second data input/output line (3), a first ferroelectric capacitor (8a) which connects the second data input/output line (3) and the first node (6), and a second ferroelectric capacitor (8b) which connects the first data input/output line (2) and the second node (7).